UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,440	11/29/2005	Peter John Miller	KILBU P-74/500728	7566

32137   7590   03/09/2009
PATENT DOCKET CLERK
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EXAMINER
GAMI, TEJAL

ART UNIT	PAPER NUMBER
2121	

MAIL DATE	DELIVERY MODE
03/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 December 2008</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-18 and 32* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-18 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This office action is responsive to an AMENDMENT entered December 23, 2008

for the patent application 10/522440.

Status of Claims

2.   Claims 1-6, 9-15, and 18 were rejected in the last Office Action dated June 26,

2008.

As a response to the June 26, 2008 office action, Applicant has Amended claims

1, 5, 6, 8-10, 14, 15, 17, and 18; Cancelled claims 2 and 11; and Added claim 32.

Claims 1, 3-10, 12-18, and 32 are now presented for examination in this office

action. 1, 3-10, 12-18, and 32

Information Disclosure Statement

3.   The prior art must be listed on a form PTO-892, PTO-1449, PTO /SB

/08A or 08B, or PTO /SB /42 (or on a form having format equivalent to one of these

forms). These forms must be properly completed. See MPEP § 2657.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 1, 3-6, 9, 10, 12-15, 18, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Ulybin (SU 1619279; Translation).

As to independent claim 1, Ulybin discloses an electronic system (e.g., electronics and computers) (see Page 3) comprising a system to be monitored having a plurality of output signals (e.g., computing system) (see Figure 1), a plurality of fault-monitoring devices (e.g., several devices) each of which is <u>adapted to</u> have a respective input from the system to be monitored and an output for outputting a fault signal (e.g., fault simulation output 13) when a respective input indicates that the system to be monitored is in a fault condition (see Page 3 and 5), wherein:

the fault-monitoring devices are arranged in a cascade fashion (e.g., cascade of several devices) and the electronic system is <u>adapted to</u> cause the first fault monitoring device of the cascade to detect a fault and to output and fault signal (e.g., fault simulating signal) such that a fault signal output (e.g., fault simulation output 13) from one fault-monitoring device is provided as an input to a subsequent fault-monitoring device in the cascade of fault-monitoring devices to simulate a fault condition associated with the subsequent fault-monitoring device (e.g., cascade fault simulation) (see Page 3 and 5), and the output of a final fault-monitoring device in the cascade is used as an indicator of a fault in one of the fault-monitoring devices (e.g., fault simulation output 13) (see Page 3 and 5).

As to independent claim 10, Ulybin discloses a self-test method (e.g., testing the fault tolerance) for an electronic system (e.g., electronics and computers) (see Page

3) comprising a system to be monitored having a plurality of output signals (e.g.,

computing system) (see Figure 1), a plurality of fault-monitoring devices (e.g., several

devices) each of which is <u>adapted to</u> have a respective input from the system to be

monitored and an output for outputting a fault signal (e.g., fault simulation output 13)

when a respective input indicates that the system to be monitored is in a fault condition

(see Page 3 and 5), the fault-monitoring devices being arranged in a cascade fashion

(e.g., cascade of several devices) and the electronic system is <u>adapted to</u> cause the

first fault monitoring device of the cascade to detect a fault and to output a fault signal

(e.g., fault simulation output 13) such that a fault signal output from one fault-monitoring

device is provided as an input to a subsequent fault-monitoring device in the cascade of

fault-monitoring devices (e.g., cascade fault simulation) (see Page 3 and 5), the method

comprising:

        inputting the fault signal from one fault-monitoring device to a subsequent fault-

monitoring device to simulate a fault condition associated with the subsequent fault-

monitoring device (e.g., cascade fault simulation) (see Page 3 and 5), wherein the

output of a final fault-monitoring device in the cascade is used as an indicator of a fault

in one of the fault-monitoring devices (e.g., fault simulation output 13) (see Page 3 and

5).

        As to dependent claim 3, Ulybin teaches an electronic system according to

claim 1, the electronic system further being arranged to:

        place the electronic system into a first fault condition and monitor for a generation

of a first fault signal from a first fault-monitoring device, on the generation of a first fault

signal from the fault-monitoring device after placing the electronic system into a first fault condition, to input the first fault signal to the second fault-monitoring device, and in response to an output from a final fault-monitoring device to store a record to this effect in non-volatile memory (see Page 14, Third Paragraph).

As to dependent claim 4, Ulybin teaches an electronic system according to claim 3 wherein, on subsequent reversion of the electronic system to a non-fault condition, the electronic system is arranged to check whether the non-volatile memory includes a record and when the non-volatile memory does not include a record on subsequent reversion (e.g., do not match), generate an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to dependent claim 5, Ulybin teaches an electronic system according to claim 1 wherein a first fault-monitoring device is adapted to output a fault signal when the electronic system is placed into a switched-off condition (e.g., with the extended non-occurrence of the tracked condition in the computing system, the condition will modify automatically) (see Page 10).

As to dependent claim 6, Ulybin teaches an electronic system according to claim 5 wherein the first fault-monitoring device is a watch-dog system (e.g., the frequency of time markers is selected so that it ensures overflow of counter 2 after the period of time specified for fault simulation at one address) (see Page 5, Second Paragraph).

As to dependent claim 9, Ulybin teaches an electronic system according to claim 1 further comprising storing a record of a fault signal output by any of the fault-monitoring devices to enable identification (e.g., address identifiers) of a defective fault-monitoring device (see Page 3).

As to dependent claim 12, Ulybin teaches a self-test method according to claim 10, further comprising:

placing the electronic system into a first fault condition and monitoring for a generation of a first fault signal from a first fault-monitoring device, on the generation of a first fault signal from the fault-monitoring device after placing the electronic system into a first fault condition, inputting the first fault signal to the second fault-monitoring device, and in response to an output from a final fault-monitoring device storing a record to this effect in non-volatile memory (see Page 14, Third Paragraph).

As to dependent claim 13, Ulybin teaches a self-test method according to claim 12 further comprising, on subsequent reversion of the electronic system to a non-fault condition, checking whether the non-volatile memory includes a record and when the non-volatile memory does not include a record on subsequent reversion (e.g., do not match), generating an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to dependent claim 14, Ulybin teaches a self-test method according to claim 10 further comprising outputting a fault signal from the first fault-monitoring device when the electronic system is placed into a switched-off condition (e.g., with the extended

non-occurrence of the tracked condition in the computing system, the condition will

modify automatically) (see Page 10).

As to dependent claim 15, Ulybin teaches a self-test method according to claim

14 wherein the first fault-monitoring device is a watch-dog system (e.g., the frequency of

time markers is selected so that it ensures overflow of counter 2 after the period of time

specified for fault simulation at one address) (see Page 5, Second Paragraph).

As to dependent claim 18, Ulybin teaches a self-test method according to claim

10 further comprising storing a record of a fault signal output by any of the fault-

monitoring devices to enable identification (e.g., address identifiers) of a defective fault-

monitoring device (see Page 3).

As to dependent claim 32, Ulybin teaches an electronic system according to

claim 1 further arranged to create a record of a fault from the output of the final-

monitoring system, the absence of a record being created signifying a fault in a fault-

monitoring device (e.g., increasing contents by "1") (see Page 13, First Paragraph).

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ulybin (SU 1619279) and further in view of Pierret et al. (U.S. Patent Number

5,079,496).

As to dependent claim 7, Ulybin teaches an electronic system according to

claim 5. Ulybin clearly teaches an electronic system, but does not mention a vehicle

ignition key. Pierre teaches electronic system is associated with a vehicle and the

electronic system is placed into a switched-off condition by turning an ignition key (see

Pierret: Col. 1, Lines 27-33). Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to have utilized a vehicle ignition key

as taught by Pierre to the electronic system of Ulybin because the closed ignition switch

enables the battery to be charged (see Pierret: Col. 1, Lines 27-33).

As to dependent claim 16, Ulybin teaches a self-test method according to claim

14. Ulybin clearly teaches an electronic system, but does not mention a vehicle ignition

key. Pierre teaches electronic system is associated with a vehicle and the electronic

system is placed into a switched-off condition by turning an ignition key (see Pierret:

Col. 1, Lines 27-33). Therefore, it would have been obvious to one of ordinary skill in

the art at the time the invention was made to have utilized a vehicle ignition key as

taught by Pierre to the electronic system of Ulybin because the closed ignition switch

enables the battery to be charged (see Pierret: Col. 1, Lines 27-33).

8.   Claims 8 and 17are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ulybin (SU 1619279) and further in view of Aslin et al. (U.S. Patent Number 4,943,919).

As to dependent claims 8 and 17, Ulybin teaches an electronic system. Ulybin

clearly teaches a second fault-monitoring device has as an input the fault signal from

the first fault-monitoring device, the second fault-monitoring system being adapted to

output a fault signal (see Ulybin: Page 3), but does not mention an under- or over-

voltage condition. Aslin teaches an electronic system experiencing an under- or over-

voltage condition (see Aslin: Col. 12, Lines 38-41). Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to have

utilized voltage condition as taught by Aslin to the fault-monitoring system of Ulybin

because the analog discrete fault data is analyzed in the same manner as the digital

fault data (see Aslin: Col. 12, Lines 47-49).

Response to Arguments

9.   Applicant's amendment and arguments filed December 23, 2008 for claims

Elected have been fully considered. The amendment does not overcome the original

art rejection and the arguments are not persuasive. The following are the Examiner's

observations in regard thereto.

Applicant Argues:

Therefore, rather than detecting an unexpected fault occurring in a system's normal course of operation
as recited in the present application, Ulybin purposely creates a faulty calculation product by inserting a
fault signal at a predefined memory location within a computing system performing the calculation.

Examiner Responds:

Examiner is not persuaded. Applicant's specification discloses a self-test system and

claims recite "simulate a fault condition". The claims and only the claims form the metes

and bounds of the invention. The Examiner has full latitude to interpret each claim in

the broadest reasonable sense. Therefore, limitations cannot be read into the claims for

the purpose of avoiding the prior art; see In re Sprock, 55 CCPA 743, 386 F.2d 924, 155

USPQ 687 (1968).

Applicant Argues:

Therefore, while Ulybin does discloses a cascade of fault insertion devices which provides an accurate
identification of a fault insertion address, it does not disclose a means of cascade of fault insertion
devices which provides a means of determining whether there is a fault with any one of the fault insertion
devices within the cascade.

Examiner Responds:

Examiner is not persuaded. The claims and only the claims form the metes and bounds

of the claims. Therefore, limitations cannot be read into the claims for the purpose of

avoiding the prior art; see In re Sprock, 55 CCPA 743, 386 F.2d 924, 155 USPQ 687

(1968). The fault insertion of the prior art is an "indicator" a fault condition using a daisy-

chained fault signaling system. Under such consideration, the claims as written are

anticipated by the prior art.

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

        Jacobson (U.S. Patent Number: 7,035,834) teaches a engine control system

using a cascaded neural network.

        Provan et al. (U.S. Patent Number: 6,208,955) teaches distributed maintenance

system based on casual networks.

11.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tejal J. Gami whose telephone number is (571) 270-1035. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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